



USER MANUAL

TriMag™

**Triple Track MagStripe
Decoding ASIC**

ICC178R

**80053501-001-C
09-4-2013**

TriMag MagStripe Decode ASIC

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TriMag MagStripe Decode ASIC

1.0 Introduction

The TriMag ASIC is a complete, three tracks MagStripe data decoder with internal memory and industry standard interfaces. TriMag ASIC provides three identical F2F decoding channels. TriMag amplifies read head signals and decodes the signal into a digital data format. The decoded signal is buffered into internal ASIC memory. TriMag has two data output formats, Clock & Data for each track or a full-duplex SPI.

Signal amplitudes from magstripe read heads can range from 3mVpp to 1Vpp; the TriMag automatic gain control operates over this range and has a fast adaptation algorithm, which compensates for magnetic signal variations caused by magnetic or mechanical stripe damage. TriMag easily decodes F2F data rates from 200 to over 42,000 data indices per second translating to media speeds from 3 to 100 inches per second. The powerful decoding algorithms compensate for typical decoding problems like dropout, skew, low amplitude, jitter, stripe noise, and magnetic bias. The Clock & Data outputs are buffered and available at real-time data rates or half time data rates. The SPI port transfers the buffered data at the SPCK rate.

TriMag is a fully contained, fully functional electronic decoding component. The only external component required is decoupling capacitance for power supply input(s).

1.1 General Features

- State of the art mixed signal, Application Specific IC (ASIC)
- Compact, standard IC package, TSSOP-20 pin
- Simultaneously decodes and buffers three magnetic stripe tracks
- Easily decodes standard 75 & 210 BPI decoding for used cards
- Reads data from card swipe speeds from 3 to 100 IPS
- Supports two power supply voltages 3.0V to 3.6V or 4.5V to 5.5V
- Operating temperature range from -40°C to +85°C
- Low power sleep mode current <80µA with 3V supply
- Low power operation during read decoding <3mA
- Two options for card data output are provided, SPI or individual Clock & Data
- Card Present or SPI Status Byte for indication of MagStripe data
- Automated internal head compensation to support most head types
- Automatic Gain Control for magnetic signal range from 3mV to 1V
- Simple to integrate & cost effective decoding solution
- High immunity to ambient noise and electrostatic discharge

TriMag MagStripe Decode ASIC

1.2 Abbreviations

AFR	Annual Failure Rate
AGC	Automatic Gain Control
ESD	Electrostatic Discharge
mA	milli-Amperes
MISO	SPI Master in Slave Out data line
MOSI	SPI Master Out Slave In data line
MSRD	MagStripe Reader Data
MTBF	Meat Time Between Falure
PCB	Printed Circuit Board
POH	Power On Hours
RAM	Random Access Memory
SPCK	SPI Clock signal line
SPI	Serial Peripheral interface
Ta	Ambient Temperature
Tj	Junction Temperature
Tjmax	Maximum Junction Temperature
Tlead	Lead Temperature
Tslew	Input Slew Rate
TSSOP	Thin-Shrink Small Outline Package
VDD	Supply voltage that corresponds to a logic 1 rail.
Vil	Voltage input low, representative of a logic 0 at an input.
Vih	Voltage input high, representative of a logic 1 at an input.
Vol	Voltage output low, representative of a logic 0 on an output.
Voh	Voltage output high, representative of a logic 1 on an output.
VSS	Supply voltage that corresponds to a logic 0 rail. Typically 0V
uA	micro-Amperes

2.0 Operating Parameters and Conditions

The ASIC has two interface modes. The interface mode is selectable. One mode is a standard, real-time MagStripe Reader Data (MSRD) (a.k.a. Clock & Data) interface. The other mode is a standard Serial Peripheral Interface (SPI) interface in slave operation.

The MSRD interface has seven signals. There is a Data output and a corresponding Clock output for each magnetic stripe track input. There is a single Media Detect output common to the three decoding circuits. The timing of the MSRD mode is shown in the timing diagram. There are two selectable clock speeds. Clock speed is selected to be the same rate as card data read rate or half of the card data read rate.

The TriMag can provide data output as an SPI slave mode. The SPI interface receives commands from the application and sends buffered magnetic stripe data to the application via the SPI Data Out pin.

TriMag MagStripe Decode ASIC

2.1 Recommend Operation Conditions

TriMag is powered by either a 5V or a 3V volt supply. When powered by a 5V supply, the VDD_IO pin is tied to 5V supply and a 0.1µf decoupling capacitor. The VDD_3V pin is tied to a 0.1µf decoupling capacitor used for an internal regulator circuit.

When powered by a 3V supply, the VDD_IO pin and VDD_3V pin are tied together to the 3V supply and a 0.1µf decoupling capacitor. See Section 4 for ASIC Pin-outs, Schematics, & Layout Recommendations.

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the ASIC outside the operating ranges may cause damage to the device or produce erratic operation. Operating outside the recommended operating ranges for extended periods may affect device reliability.

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V _{dd_5V}	5V DC Supply	4.5	5.5	V	(1)
V _{dd_3V}	3V DC Supply	3.0	3.6	V	(2)
I _{ddd}	Dynamic Current		3.0	mA	(3)
I _{dds5}	Standby Current (sleep)		85	uA	5V mode(4)
I _{dds3}	Standby Current (sleep)		80	uA	3V mode(4)
A _{vss}	Analog Ground		0	V	
D _{vss}	Digital Ground		0	V	
T _a	Ambient Temperature	-40	85	C	
T _j	Junction Temperature	-40	90	C	(5)

Figure 1 Operating Parameters

Notes:

1. TriMag is operated in a single voltage mode, either 5V or 3V.
2. If 3V mode is used, the 5V supply is externally tied to the 3V supply.
3. Dynamic current is with oscillator running, all analog cells out of power down mode, and digital cells running a calculation. All outputs unloaded. All inputs are driven & not floating.
4. Standby current is with the low frequency clock powering the signal detect and wake-up circuits. All other analog cells are in power down and all other digital logic are powered up with no clocks running. All outputs are unloaded and inputs are tied high or low. No inputs are floating. There is No SPI activity.
5. TSSOP Theta-J is 118.6 deg C/W for single-sided board with no ground plane

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2.2 Absolute Maximum Ratings

Stresses above those listed in this section may cause immediate device failure.

SYMBOL	PARAMETER	MIN	MAX	UNITS
V _{dd_5V}	5V DC Supply Voltage	-0.3	6	V
V _{dd_3V}	3V DC Supply Voltage	-0.0	3.7	V
V _{in_5V}	Input Pin Voltage, 5V mode	VSS-0.3	VDD_5+0.3	V
V _{in_3V}	Input Pin Voltage, 3V mode	VSS-0.3	VDD_3+0.3	V
I _{in}	Input Pin Current	-10	10	mA
T _{strg}	Storage Temperature	-55	150	C
T _{lead}	Lead Temperature	N/A	260	C
ESD	Direct contact ESD	–	4	KV
Capacitive Load	The parasitic capacitance at outputs driven @19kHz	–	50	pF

Figure 2 Absolute Maximum Ratings

2.3 DC Operating Conditions

Pin	Name	TYPE	V _{il} (max) Volts	V _{ih} (min) Volts	I _{il} (min/ max) uA	I _{ih} (min/ max) uA	V _{ol} (max) Volts	V _{oh} (min) Volts	I _{ol} (max) mA	I _{oh} (max) mA
7	MSR (SPI)	IN	0.3*Vdd	0.7*Vdd	1μA	1μA				
8	nCS	IN	0.3*Vdd	0.7*Vdd	1μA	1μA				
9	CK1	OUT					0.4V	0.8*VDD	-4/8mA	4/8mA
10	DA1	OUT IN	0.3*Vdd	0.7*Vdd	1μA	1μA	0.4V	0.8*VDD	-4/8mA	4/8mA
11	CK2	OUT					0.4V	0.8*VDD	-4/8mA	4/8mA
12	DA2	OUT IN	0.3*Vdd	0.7*Vdd	1μA	1μA	0.4V	0.8*VDD	-4/8mA	4/8mA
13	CK3	OUT IN	0.3*Vdd	0.7*Vdd	1μA	1μA	0.4V	0.8*VDD	-4/8mA	4/8mA
14	DA3	OUT IN	0.3*Vdd	0.7*Vdd	1μA	1μA	0.4V	0.8*VDD	-4/8mA	4/8mA
15	MD / MISO	OUT					0.4V	0.8*VDD	-4/8mA	4/8mA
16	PRO / SPCK	IN	0.3*Vdd	0.7*Vdd	1μA	1μA				
17	MOSI	IN	0.3*Vdd	0.7*Vdd	1μA	1μA				

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2.4 External Component Parameters

These component parameters apply to the minimum ASIC circuit configuration. Other components may be used for extended noise or ESD immunity. Contact ID TECH Support for additional information.

Component	Function	Nominal Value	Tolerance	Units
Capacitor	Required decoupling capacitor for 3.3V or 5V applications	0.1	-20%, +20%	μ F
Capacitor	Required decoupling only when used in 5V application	0.1	-20%, +20%	μ F
Head Inductance	Head Inductance (per track)	100	+30 -60	mH (at 1kHz, 100 μ A RMS)
Head Resistance	Head DC Resistance (per track)	280	+/-30	Ohms

Figure 3 External Component Values

2.5 Component MTBF & ARF

The device MTBF is 2,200,000 POH having an AFR of 0.398% with a 90% confidence.
The device MTBF is 5,500,000 POH having an AFR of 0.159% with a 60% confidence.

TriMag MagStripe Decode ASIC

3.0 General Functional Description

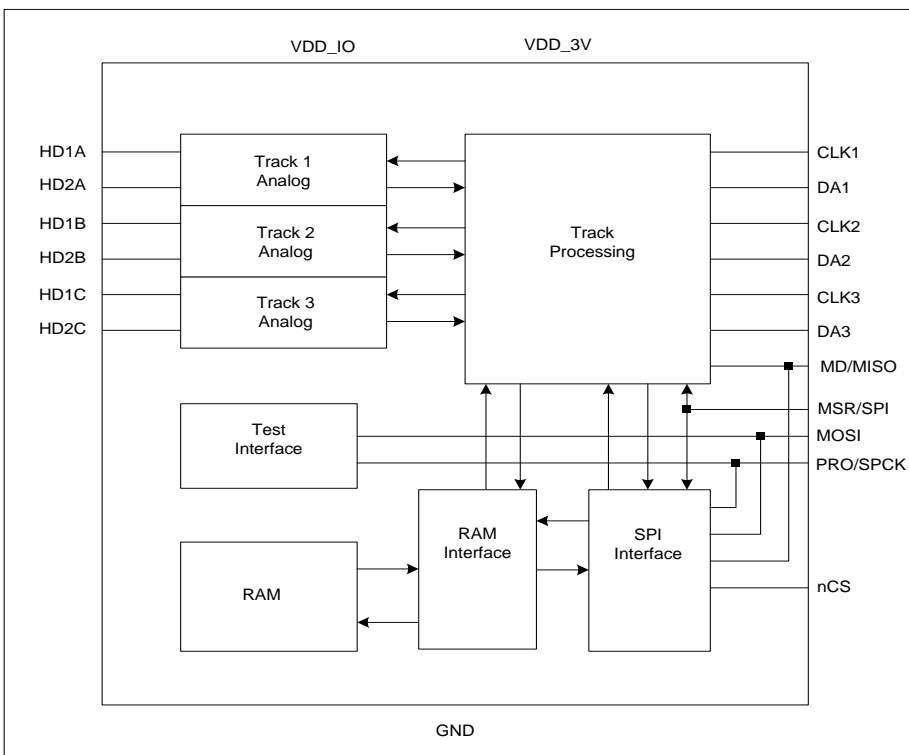


Figure 4 ASIC Architectural Block Diagram

3.1 General Functional Description

Three analog sections process the incoming head signals. Each section contains a signal filtering and noise reduction elements. Each analog section interfaces to an identical digital section that monitors the amplitude of the recovered analog signal and provides AGC settings and bandwidth adjustments. The analog sections have sophisticated peak detection for signals representing the recorded data bits. Digital circuits delineate the data bit stream and store the bit values in internal RAM storage.

The TriMag ASIC has two primary data output modes, Magnetic Stripe Reader Data (MSRD) mode, and SPI mode. In either mode, the recovered data is stored RAM and is output through the chosen data interface.

In MSRD mode, data is provided through three traditional Clock & Data outputs. The Clock & Data information is captured by an external processor. A valid level on the Media Detect pin indicates the reading process.

In SPI mode, an external processor communicates with the RAM via the SPI interface to retrieve the decoded track data. SPI commands & status control the interface operation.

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3.2 Sleep Mode Function

TriMag will automatically enter a power-down sleep mode when a magnetic head signal is not present. The MagChip will automatically wake-up when a magnetic head signal is present. The outputs Data, Strobe, & Media Detect are at a high level during sleep mode.

3.3 MSRD Mode Outputs

3.3.1 Data Output

The Data output is a serial stream of digital bits, which are the decoded information from the magnetic stripe media (card). The bit level of the Data output, with the corresponding strobe (Clock), represents each Data bit that was recorded on the magnetic strip track. The first 6 to 9 bits (after Wake-up) from the leading edge of a magnetic stripe are not provided as output; these bits are used for circuit synchronization. A Data output high level is a 'ZERO' value data bit and a low level is a 'ONE' value data bit. The Data output matches the card data when media is moved by the head in a forward direction. The Data output is a mirror image of card data when media is moved by the head in a reverse direction.

3.3.2 Data Strobe (Clock) Output

The Data Strobe is a clocking output indicating the magnetic data bit value is present at the Data output. The Strobe output is normally high and goes low to indicate the start of a data sample time. The Data output is stable and may be sampled on the falling or rising edge of Data Strobe, or at anytime within a window defined by the card speed and media data density. The receiving interface for the magstripe Data must sense the Hi to Lo Strobe transition (leading edge) and acquire the Data bit level within a time not exceeding the timing of the next Clock output. Since the MagStripe data is buffered into RAM, the Clock output is NOT synchronized real time with the card speed & data density like found in previous versions of decoding ASIC. A Half Clock timing mode is selectable to allow data retrieval at a slower rate.

3.3.3 Media Detect Output

This output indicates the presence of recorded magnetic media passing the read head on at least one card data track. This signal is normally high impedance; a low output indicates media. The output is an open drain type. A pull-up resistor is needed for proper operation when used. The Media Detect output occurs after circuit synchronization, which is the detection of six consecutive & consistent zero bits are from any one track. After Media Detect is low, there is a $3\mu\text{S} \pm 50\%$ delay before the first Data Strobe (Clock) output.

Note: The track designations are based on read head location to the card reference surface in the reader. The head connections for the MagStripe tracks match the head wires associated with the magnetic stripe tracks. The three decoding channels in the ASIC are identical; any head track signal can be applied to any track pins input pair. The outputs will provide the decoded data from the applied inputs.

TriMag MagStripe Decode ASIC

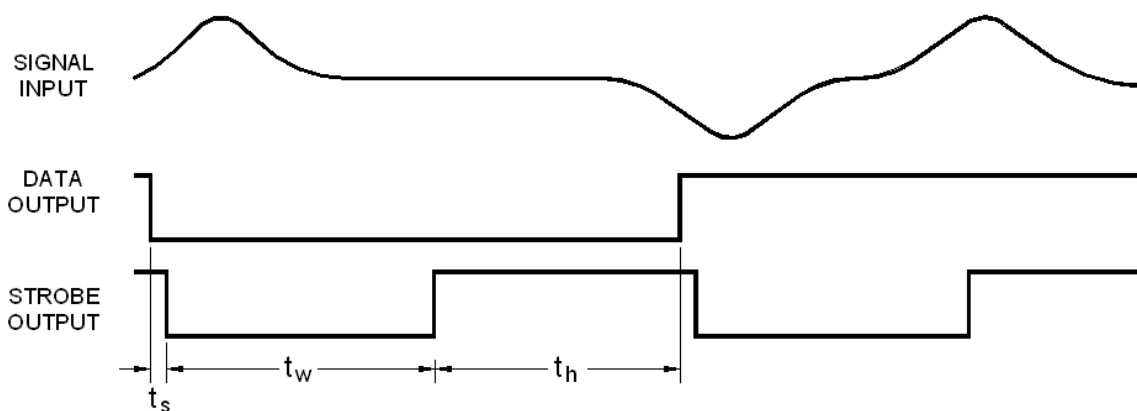


Figure 5 Clock and Data Timing Diagram

Symbol	Parameter	Timing
t_s	Setup Time, DATA Change to STROBE Falling Edge	$3\mu\text{S} \pm 50\%$
t_h	STROBE Rising Edge to DATA Change*	50% of bit width $\pm 3\mu\text{S}$
t_w	Pulse Width, STROBE*	50% of bit width $\pm 3\mu\text{S}$

Figure 6 Clock and Data AC Characteristics

* The Clock & Data output width is doubled when PRO control pin (Pin-16) is connected to power supply common. This feature allows for slower data acquisition timing for low speed microprocessors.

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3.4 SPI Mode Operation & Outputs

The SPI operation implements a common SPI slave-only interface. Although there are many permutations of SPI, the TriMag offers only a single communication format. This format is the most common. Its characteristics are as follows:

- Input data is latched on the rising edge of the serial clock
- Output data is shifted out on the falling edge of the serial clock
- SPI is enabled when nCS is low
- Output data is tri-stated when SPI is not enabled (nCS is high)
- The maximum SPI clock rate is less than 500 kHz ensuring memory reads have sufficient time to complete for back-to-back SPI reads.

These relationships are shown below for a simple 8-bit command, followed by an 8-bit response.

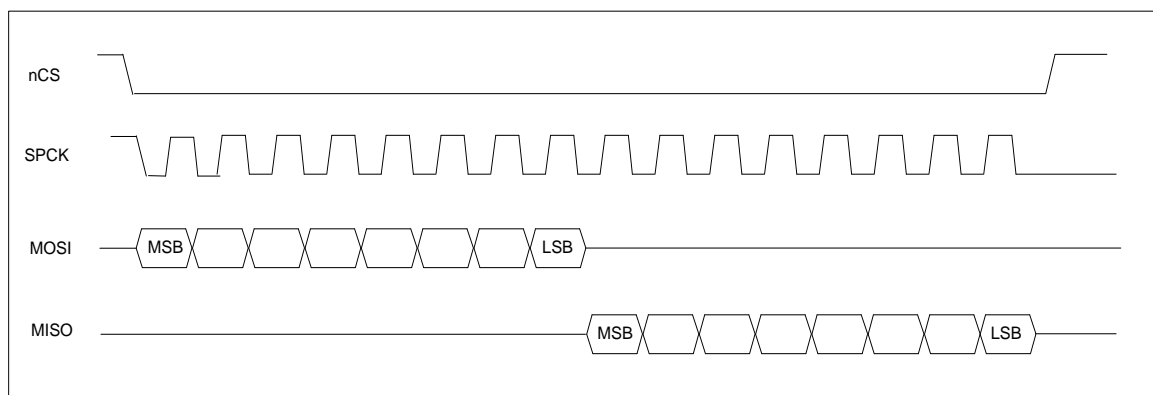


Figure 7 SPI Communication Timing Diagram

3.4.1 Static RAM Buffer

Decoded data is buffer in a single 2304 x 1 single port static RAM. The RAM is used as three 768-bit buffers. One buffer is used for each MagStripe track. Data from the Track 1 head input is saved in locations 0x000 through 0x2FF, data from the track 2 head input is saved in locations 0x300 through 0x5FF, and data from the track 3 head input is saved in locations 0x600 to 0x8FF.

The decoded leading and trailing Zero bits (synchronization bits) are saved in the RAM along with the data bits. The processor must ignore the synchronization bits and format the data characters using pattern matching and parsing techniques.

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3.4.2 SPI Normal Mode Operation

The SPI interface is primarily for reading the contents of the RAM to retrieve the MagStripe data. The SPI data block is preceded by a header, and is followed with a validation byte consisting of a Longitudinal Redundancy Check (LRC), which is computed as a bit-wise XOR across all previous data bytes.

The header byte consists of several status bits.

- Bit 0 This is the “Busy” bit. When bit is high, it signals that the RAM is busy with an active swipe.
- Bit 1 This is the “Empty” bit. When it is high, it signals that the RAM is currently empty. If the RAM is busy or empty, only the header is returned to the host. There is no data and no LRC in this case. The header status is set to not busy & not empty after a new swipe is detected & while old buffer data is erased.
- Bit 2 This is the “Power on Reset” (POR) bit, and when high it signals that a POR event has occurred. This bit is cleared immediately after reading.
- Bit 6 This is an “Error” bit indicating an invalid (not recognized) command was given.
- Bit 7 This is an “Out of Order” bit indicating a command was given out of order and could not be serviced. The Error & Out of Order bits are cleared immediately after they have been read or after an ATR or a POR event.

The normal sequence is for the processor (SPI Master) to read the data blocks in a looping construct (polling). When all magnetic data is reported in the RAM, the magstripe data is transferred from TriMag. The Busy & Empty bits provide the status.

Bit 0	Bit 1	Status Description
0	0	Data in RAM & Ready to read
0	1	No data available
1	0	Magstripe read in progress
1	1	Same as, Magstripe read in progress

SPI commands are shown in the table below. For all commands, the SPI interface logic counts SPCK transitions while nCS signal is low. A command counter uses eight clock edges to capture the command word and decode it. A transition on nCS resets the count.

If the implementation has nCS chip select tied low at all times. A timeout is provided to reset the command counter. The timeout is approximately 64 milliseconds and is active even in sleep mode. Activity on the SPI_CLK line resets the timeout.

The SPI supports a dedicated command to flush the RAM. All three buffers are erased in one operation. This process is clocked by the master system clock, and is completed in 2304 cycles, plus a few more to initiate the operation. This timing is less than one millisecond. When the erase is initiated, the data read header status changes to indicate the RAM is busy. When the erase is finished, the status is changed to empty.

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When any read request is made that does not return the “busy” or “empty” flag, the SPI initiates a “transaction” and receives exclusive access to the RAM. The “transaction” ends when the “Arm to Read / Flush RAM buffer” command is given. Any new card swipe made during a “transaction” is ignored. Any new read made during a “transaction” is also ignored and the out-of-order error bit is set.

3.4.3 SPI Operational Command Descriptions

Serial Command	Action	Serial Output
0x01	Read track one data sequentially	Header, Track 1 data, LRC
0x02	Read track two data sequentially	Header, Track 2 data, LRC
0x03	Read track three data sequentially	Header, Track 3 data, LRC
0x04	Read all tracks sequentially	Header, Track one data, Track two data, Track three data, LRC
0x05	Arm to Read / Flush RAM buffer	0x05
0x06	Report Status	Header
0x11	Byte read track one data	Header
0x12	Byte read track two data	Header
0x13	Byte read track three data	Header
0x14	Byte read all track data	Header
0x15	Continue reading data	Data or LRC (see below)
0x16	End of Cycle / Reset	None
0x00 or 0xFF (preferably 0xFF)	NoOp	Empty, unless in sequential read, in which case the read continues unaffected

Figure 8 SPI Communication Commands List

Note: The track designations are based on read head location to the card reference surface in the reader. The head connections for the MagStripe tracks match the head wires associated with the magnetic stripe tracks. The three decoding channels in the ASIC are identical; any head track signal can be applied to any track pins input pair. The outputs will provide the decoded data from the applied inputs.

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3.4.4 Sequential Reads Vs Byte Reads

When reading a track (or all tracks) sequentially, as long as the nCS (SPI Chip Select) is asserted and the SPI clock is toggling, data is sent to the master. During this time, the incoming instructions should be "NoOp's (the number of data bytes, n, plus 2). For example, when reading one track, the entire data are streamed out in one $1+96+1=98$ -byte block (784 bits). When reading the entire buffer, the message length is $1 + 3*96 + 1 = 290$ bytes (2320 bits). If the host continues to clock out data after the end of the LRC, empty (0xFF) is transmitted.

A byte read is different. The initial read command returns the header information. If the RAM is not busy & not empty, then the host follows with multiple "Continue reading data" commands (n+ 1 time). Each successive "Continue" command returns the next byte of data, until the last byte. After the last byte is received, a NoOp command is sent while the LRC is received. If an extra continue command is issued, the out-of-order error bit is set but the LRC byte is still received on the (n+2) cycle. Further "Continue" commands return empty (0xFF) and the out-of-order error bit is set. If another command is issued during the (n+2) cycle while the LRC byte shifts out, that command is serviced normally.

If a new status or read command is issued before the data has been completely read, the new read process is ignored, the error bit is set, and data (for a sequential read) or empty (for a byte read) is returned as if a NoOp had been issued. The exception is that if a status or read command is sent while a header is being sent out, no error would be set. This is because the host cannot know the header was valid (or not) and that a read began until it receives the header. If this is the case, the host issues one fewer NoOp (n+1) or Continue (n) commands to stream out all data.

EOC and ATR have the same priority. This is the second highest priority. They can interrupt all other modes. Issuing the "Reset" (EOC) command ends the read process early without setting the error status bit. The "Arm to Read" (ATR) commands exits the read, erase the memory, and returns the SPI to an idle state, with all error bits cleared. De-asserting the chip select signal aborts all SPI commands and return to an idle state with all error bits cleared.

TriMag MagStripe Decode ASIC

4.0 TriMag Physical Information

4.1 Pin I/O Descriptions

Pin #	Name	Pad Description
1	HD1	Magnetic head input, track 1
2	HD1	Magnetic head input, track 1
3	HD2	Magnetic head input, track 2
4	HD2	Magnetic head input, track 2
5	HD3	Magnetic head input, track 3
6	HD3	Magnetic head input, track 3
7	MSRD SPI	MSRD mode: connect to VDD_5V SPI mode: connect to GND
8	nCS	MSRD mode: not used (tie low) SPI mode: SPI chip select
9	CK1	MSRD mode: Track1 CLK
10	DA1	MSRD mode: Track1 DATA
11	CK2	MSRD mode: Track2 CLK
12	DA2	MSRD mode: Track2 DATA
13	CK3	MSRD mode: Track3 CLK
14	DA3	MSRD mode: Track3 DATA
15	MD MISO	MSRD mode: Media Detect, Open drain SPI mode: Slave Out, Normal Hi - Z
16	PRO SPCK	MSRD mode: PRO = 0: Date rate = ½ card speed rate PRO = 1: Date rate = card speed rate SPI mode: SPI interface clock
17	MOSI	MSRD mode: not used (tie low) SPI mode: Slave input data
18	VDD_3V	3V operation: connect to 3.3V supply voltage 5V operation: connect regulator decoupling capacitor
19	VDD_IO	3V operation: connect to 3.3V supply voltage* 5V operation: connect to 5V supply voltage*
20	GND	Ground connection

Figure 9 ASIC Pin-Out List

* The supply voltage must always have a decoupling capacitor.

TriMag MagStripe Decode ASIC

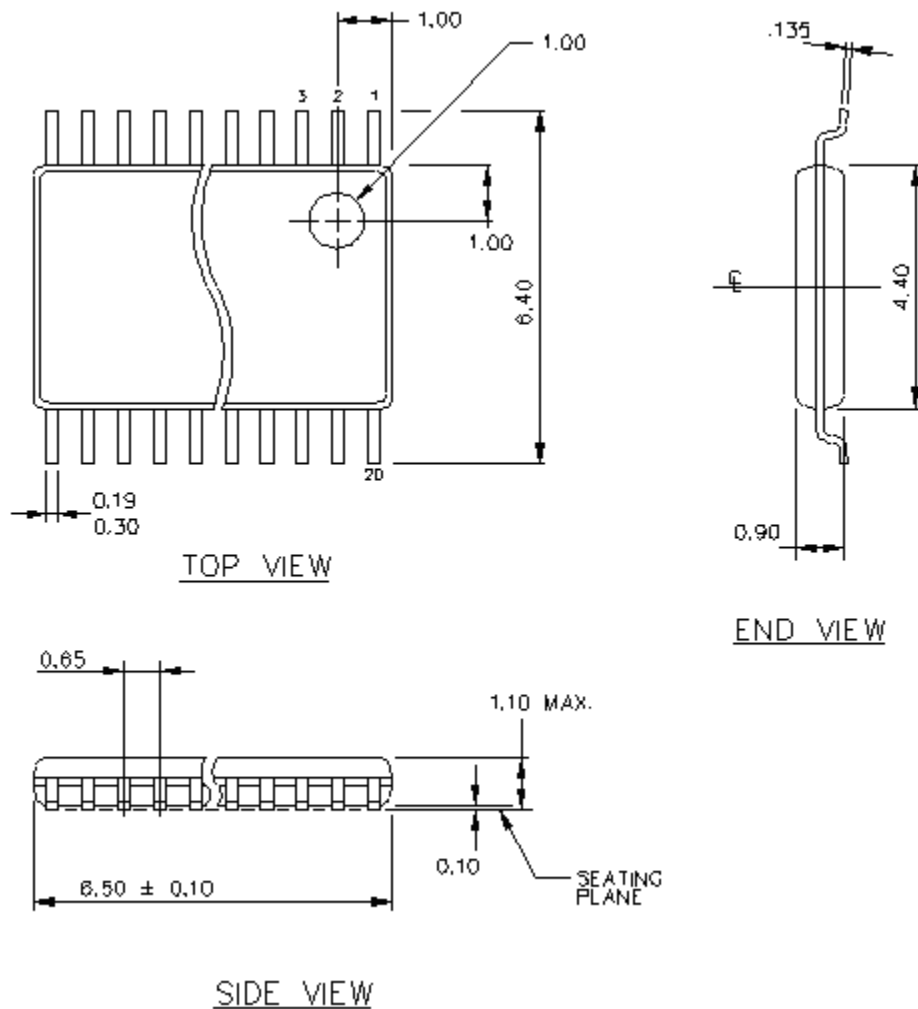


Figure 10 ASIC Package & Pin Assignment Drawing

The TriMag brand name and a manufacturing data code are printed on the ASIC package. TriMag is a RoHS compliant component.

TriMag MagStripe Decode ASIC

4.2 Schematic Diagrams

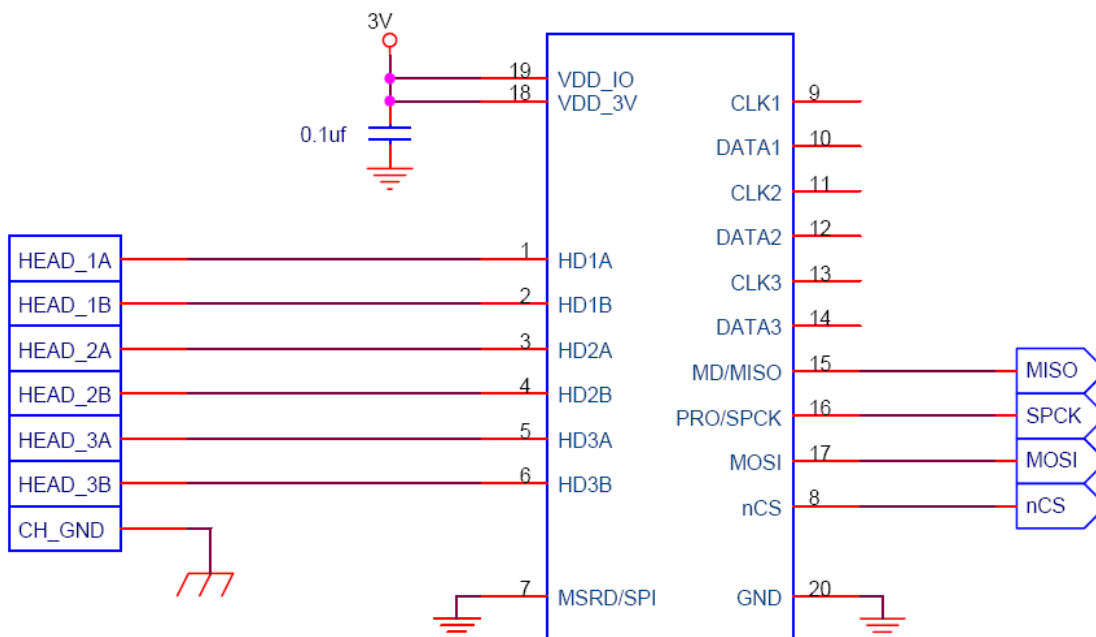


Figure 11 Schematic Diagram, SPI w/ +3.3V supply

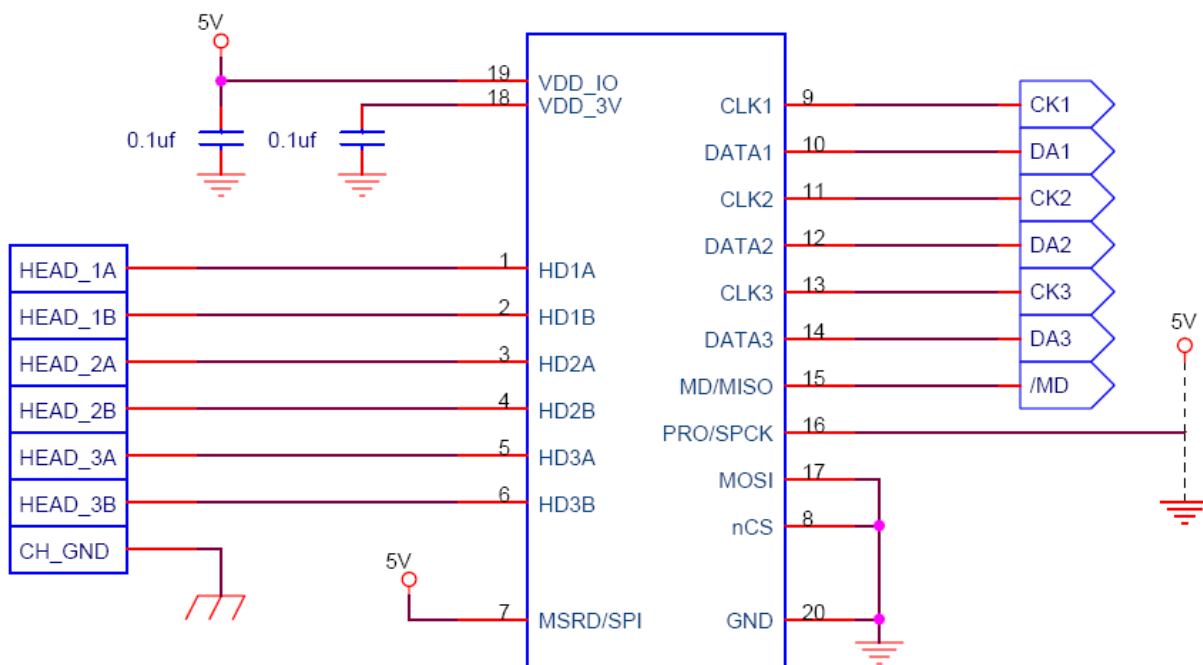


Figure 12 Schematic Diagram, Clock & Data w/ +5V supply

TriMag MagStripe Decode ASIC

4.3 PCB Layout Suggestions

The PCB layout should keep the head input signals lines as short as possible and separated from the digital outputs to minimize external noise pick-up and digital to analog cross talk. Pin 1 is denoted with a dot in the package corner next to pin 1.

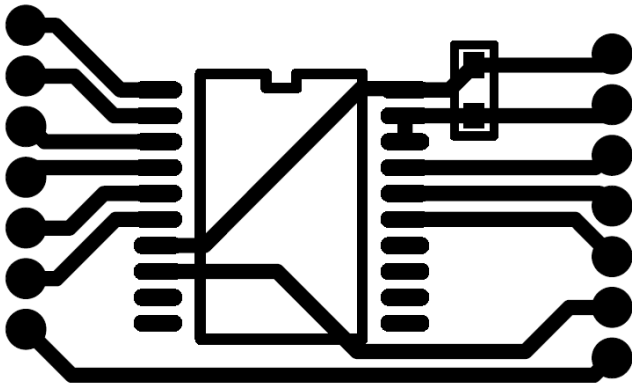


Figure 13 PCB layout Recommendation +3.3V operation

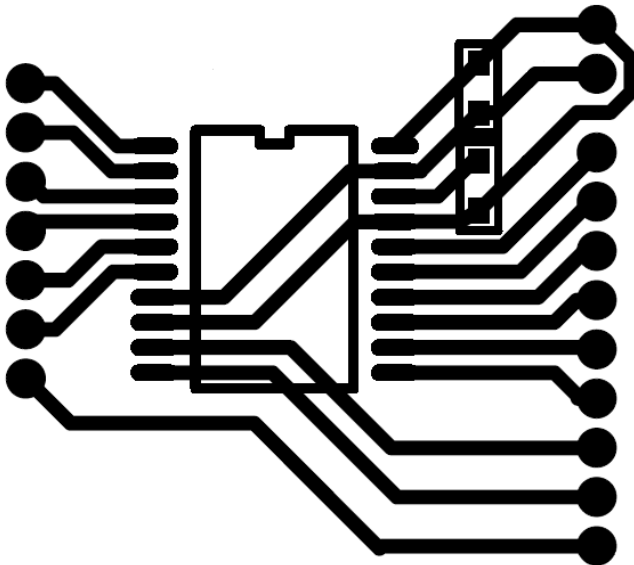


Figure 14 PCB layout Recommendation +5V operation